Ver 2.0

5GHz Radiation hardened wideband integer-N frequency synthesizer

Datasheet

Part Number：BM7101MQRH

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1.0	2017/04/05		Initial Revision	
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1. Features

- **Scrubbing features**
  - Programmable dual-modulus prescaler: 8/9, 16/17, 32/33, 64/65
  - Programmable antibacklash pulse width
  - Hardwired programmable
  - Digital lock detect
  - Hardware power-down mode
  - Without internal register
  - Package: CQFP48
- **Electrical characteristics**
  - 3.0V to 3.6V supply voltage
  - RF input frequency range : 0.5GHz ~ 5GHz
  - Reference input frequency range : 10MHz ~ 200MHz
- **Reliability features**
  - Operating temperature : -55℃ ~ +125℃
  - ESD (human body model) : 2000V
  - Total ionizing dose : ≥ 100Krad(Si)
  - Single event latch-up threshold : ≥75MeV·cm^2/mg

2. General Description

The BM7101MQRH frequency synthesizer can be used to implement local oscillators in the up-conversion and down-conversion sections of wireless receivers and transmitters. It consists of a low noise, digital phase frequency detector (PFD), a precision charge pump, a programmable reference divider, programmable A counter and B counter, and a dual-modulus prescaler (P/P + 1). The A (4-bit) counter and B (10-bit) counter, in conjunction with the dual-modulus prescaler (P/P + 1), implement an N divider (N = BP + A). In addition, the 6-bit reference counter (R Counter) allows selectable REF_{IN} frequencies at the PFD input. A complete phase-locked loop (PLL) can be implemented if the synthesizer is used with an external loop filter and voltage controlled oscillator (VCO). It's very high bandwidth means that frequency doublers can be eliminated in many high frequency systems, simplifying system architecture and reducing cost.

3. Function Block Diagram

BM7101MQRH function block diagram is shown in figure 3-1.

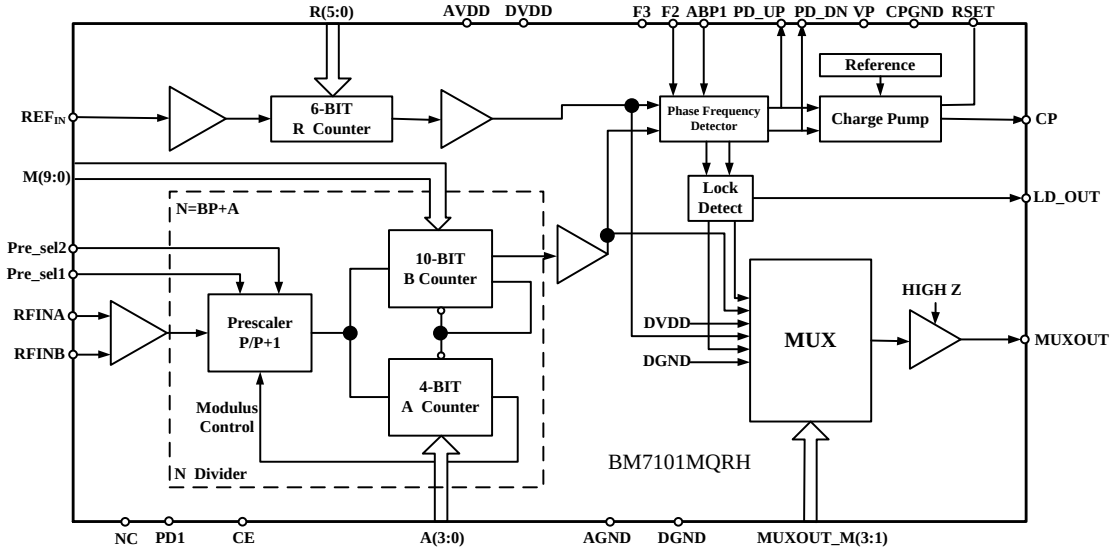

Figure 3-1 BM7101MQRH function block digram

4. Packages and Pin Function Descriptions

The provided package is: CQFP48.

BM7101MQRH CQFP48 pin configuration is shown in 4-1, in top view the pin P1 is in the bottom of the left side, the pins are arranged in anticlockwise order.

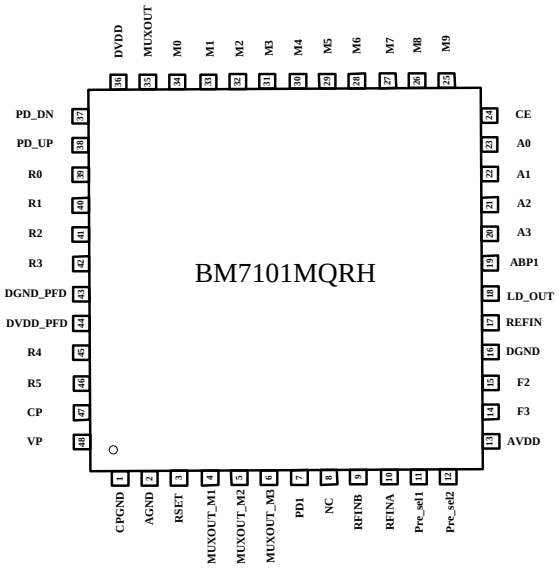

Figure 4-1 CQFP48 pin configuration

Talble 4-1 BM7101MQRH Pin Function Descriptions

Pin No.	Terminal Symbol	Pin Type	Function	Pin No.	Terminal Symbol	Pin Type	Function
1	CPGND	GND	Charge pump Ground	25	M9	I	B Counter Bit9
2	AGND	GND	Analog Ground	26	M8	I	B Counter Bit8
3	R_{SET}	I/O	Bias for charge pump	27	M7	I	B Counter Bit7
4	MUXOUT_M1	I	MUXOUT Control	28	M6	I	B Counter Bit6
5	MUXOUT_M2	I	MUXOUT Control	29	M5	I	B Counter Bit5
6	MUXOUT_M3	I	MUXOUT Control	30	M4	I	B Counter Bit4
7	PD1	I	Power Down1	31	M3	I	B Counter Bit3
8	NC	I	NC	32	M2	I	B Counter Bit2
9	$RF_{IN}B$	I	Complementary Input to the RF Prescaler	33	M1	I	B Counter Bit1
10	$RF_{IN}A$	I	Input to the RF Prescaler	34	M0	I	B Counter Bit0
11	pre_sel1	I	Prescaler Value Control	35	MUXOUT	O	Muxtiplexer Output
12	pre_sel2	I	Prescaler Value Control	36	DV_{DD}	V_{DD}	Digital supply voltage
13	AV_{DD}	V_{DD}	Analog supply voltage	37	PD_DN	O	PFD Output
14	F3	I	CP Three-State	38	PD_UP	O	PFD Output
15	F2	I	Phase Detector Polarity Control	39	R0	I	R Counter Bit0
16	DGND	GND	Digital Ground	40	R1	I	R Counter Bit1
17	REF_{IN}	I	Reference Input	41	R2	I	R Counter Bit2
18	LD_OUT	O	Digital Lock Detect Output	42	R3	I	R Counter Bit3
19	ABP1	I	ANTIBACKLASH Pulse Width Control	43	DGND_PFD	GND	PFD Ground
20	A3	I	A Counter Bit3	44	DV_{DD}_PFD	V_{DD}	PFD supply voltage

Pin No.	Terminal Symbol	Pin Type	Function	Pin No.	Terminal Symbol	Pin Type	Function
21	A2	I	A Counter Bit2	45	R4	I	R Counter Bit4
22	A1	I	A Counter Bit1	46	R5	I	R Counter Bit5
23	A0	I	A Counter Bit0	47	CP	O	Charge pump output
24	CE	I	Chip Enable	48	VP	V_{DD}	Charge pump power supply

5. Detailed Description

5.1 Function Description

The main functions of BM7101MQRH are as follows:

1) Prescaler

T The dual-modulus prescaler (P/P + 1), along with the A counter and B counter, enables the large division ratio, N, to be realized (N = BP + A). The dual-modulus prescaler, operating at CML levels, takes the clock from the RF input stage and divides it down to a manageable frequency for the CMOS A counter and B counter. The prescaler is programmable. It can be set to 8/9, 16/17, 32/33, or 64/65. It is based on a synchronous 4/5 core. There is a minimum divide ratio possible for fully contiguous output frequencies. This minimum is determined by P, the prescaler value, and is given by (P2 − P).

pre_sel2 and pre_sel1 set the prescaler values. The prescaler value should be chosen so that the prescaler output frequency is always less than or equal to 325 MHz. Therefore, with an RF frequency of 4 GHz, a prescaler value of 16/17 is valid, but a value of 8/9 is not valid.

Talble 5-1 Pescaler Value

pre_sel2	pre_sel1	Pescaler Value
0	0	8/9
0	1	16/17
1	0	32/33
1	1	64/65

2) Power Down

PD1 provides power-down modes. It is enabled by the CE pin.

When the CE pin is low, the device is immediately disabled regardless of the states of PD1.

Talble 5-2 Power Down

CE	PD1	MODE
0	X	ASYNCHRONOUS POWER-DOWN
1	0	NORMAL OPERATION
1	1	SYNCHRONOUS POWER-DOWN

Note： When the PLL circuit is operating abnormally , the PLL circuit can be reset through the CE pin without having to return on the power.

3) MUXOUT Control

The on-chip multiplexer is controlled by MUXOUT_M3, MUXOUT_M2, and MUXOUT_M1. The table shows the truth table. The N-channel, open-drain, analog lock detect should be operated with an external pull-up resistor of 10 kΩ nominal. When lock is detected, this output is high with narrow, low-going pulses.

Caution: It is necessary to declare that, the MUXOUT output is used to test whether the circuit inside the chip is working correctly or not, and this port should be set to “Three-State Output” (MUXOUT_M3=0, MUXOUT_M2=0, MUXOUT_M1=0) to ensure the correct work of the frequency synthesizer. Otherwise, when MUXOUT is set to “R Divider Output” (MUXOUT_M3=1, MUXOUT_M2=0, MUXOUT_M1=0)、or “N Divider Output” (MUXOUT_M3=0, MUXOUT_M2=1, MUXOUT_M1=0)，the phase noise at the radio frequency output port of frequency synthesizer may deteriorate and the frequency synthesizer is likely to fail to lock at a high output frequency.

Talble 5-3 MUXOUT

MUXOUT_M3	MUXOUT_M2	MUXOUT_M1	OUTPUT
0	0	0	Three-State Output
0	0	1	Reserved
0	1	0	N Divider Output
0	1	1	DV_{DD}
1	0	0	R Divider Output
1	0	1	N-CHANNEL Open-Drain Lock Detect
1	1	0	Reserved
1	1	1	DGND

4) A counter and B counter

The A counter and B counter, in conjunction with the dual-modulus prescaler,

make it possible to generate output frequencies that are spaced only by the reference frequency divided by R. The equation for the VCO frequency is

$f_{VCO}=[(P\times B)+A]\times f_{REFIN}/R$

where:

f_{VCO} is the output frequency of the external voltage controlled oscillator (VCO).

P is the preset modulus of the dual-modulus prescaler (8/9, 16/17, etc.).

B is the preset divide ratio of the binary 9-bit counter (3 to 1023).

A is the preset divide ratio of the binary 4-bit swallow counter (0 to 15).

R is the preset divide ratio of the binary 5-bitRcounter (1 to 63).

f_{REFIN} is the external reference frequency oscillator.

Talble 5-4 A Counter

A3	A2	A1	A0	A Counter Divider Ratio
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
…	…	…	…	…
1	1	1	0	14
1	1	1	1	15

Talble 5-5 B Counter

M9	M8	M7	…	M2	M1	M0	B Counter Divider Ratio
0	0	0	…	0	0	0	Not Allowed
0	0	0	…	0	0	1	Not Allowed
0	0	0	…	0	1	0	Not Allowed
0	0	0	…	0	1	1	3
…	…	…	…	…	…	…	…
1	1	1	…	1	0	0	1020
1	1	1	…	1	0	1	1021
1	1	1	…	1	1	0	1022
1	1	1	…	1	1	1	1023

5) R counter

The 5-bit R counter allows the input reference frequency to be divided down to

produce the reference clock to the phase frequency detector (PFD). Division ratios from 1 to 63 are allowed.

Talble 5-6 R Counter

R5	R4	R3	R2	R1	R0	R Counter Divider Ratio
0	0	0	0	0	1	1
0	0	0	0	1	0	2
0	0	0	0	1	1	3
…	…	…	…	…	…	…
1	1	1	1	1	0	62
1	1	1	1	1	1	63

6) Phase Detector Polarity

This bit sets the phase detector polarity bit. When using a passive loop filter or non-inverting active loop filter, this must be set to “1”, If using an active filter with an inverting characteristic, it must be set to “0”.

Talble 5-7 Phase Detector Polarity

F2	Phase Detetor Polarity
0	Negative
1	Positive

7) Anti-backlash Pulse Width

The PFD includes a programmable delay element that controls the width of the anti-backlash pulse. This pulse ensures that there is no dead zone in the PFD transfer function and minimizes phase noise and reference spurs. ABP1 control the width of the pulse.

Talble 5-8 Anti-backlash Pulse Width

ABP1	Anti-backlash Pulse Width
0	2.9ns
1	1.3ns

8) Charge Pump Output

F3 controls the CP output pin. With the bit set high, the CP output is put into three-state. With the bit set low, the CP output is enabled.

Talble 5-9 Charge Pump Output

F3	Charge Pump Output
0	Normal
1	Three-State

9) Bias for charge pump

Connecting a resistor between this pin and GND sets the charge pump output current. The nominal voltage bias at the R_{SET} pin is 0.65 V. The relationship between I_{CP} and R_{SET} is : when R_{SET}=5.1KΩ, I_{CP}=3.0mA.

10) RF Input

The RF input stage is shown in Figure7. It is followed by a 2-stage limiting amplifier to generate the CML clock levels needed for the prescaler.

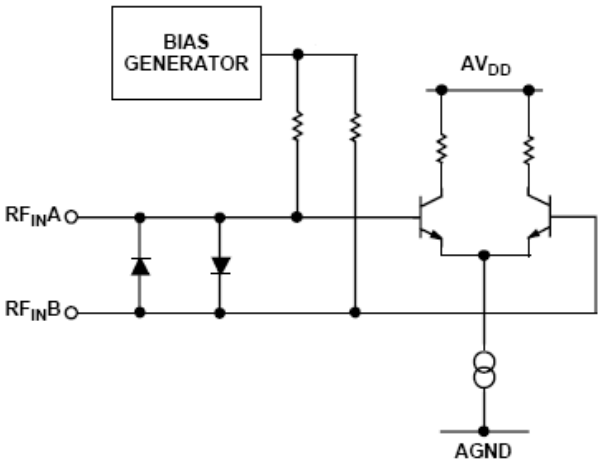

Figure 5-1 RF input stage

11) PFD Output

The phase detector is triggered by rising edges from the A/B counter(fp) and the reference counter(fc). It has two outputs namely PD_UP and PD_DN. PD_UP and PD_DN are designed to drive an active loop filter which controls the VCO tune voltage.

12) Lock Detect

When the PLL is in lock, the digital lock detect LD_OUT is open-drain output, otherwise LD_OUT is a logic low(“0”). When five consecutive cycles of less than 15ns pulse width are detected, the LD_OUT is set to high. It stays set high until a phase error of greater than 25ns is detected on any subsequent PFD cycle. When pulse width of LD_in is bigger than 15ns and smaller than 25ns, LD_OUT keeps lock state, and the lock detect circuit is disabled to reduce power consumption.

5.2 Storage Condition

Packaged product should be stored in the ventilate warehouse with ambient temperature 10℃～30℃ and relative humidity less than 70%. There should be no acid , alkali or other radiant gas in the environment.

5.3 Absolute Maximum Ratings

a) Supply voltage (AV_{DD}、DV_{DD}、DV_{DD}_PFD、V_P) : -0.3V ~ 3.9V
b) Voltage on any input (V_I) : -0.3 V ~ V_{DD}+0.3V
c) Operation temperature range (T_A) : -55℃ ~125℃
d) Storage temperature range (T_{stg}) : -65℃ ~ 150℃
e) Maximum Junction Temperature (T_J) : 150℃
f) Thermal resistance ($R_{th(J-C)}$) : 5℃/W
g) Lead Temperature 10s (T_H) : 260℃

5.4 Recommended Operation Conditions

a) Supply voltage (AV_{DD}、DV_{DD}、DV_{DD}_PFD、V_P) : 3.0V ~ 3.6V
b) Operation temperature range(T_A) : -55℃ ~ 125℃

6. Specifications

All electrical characteristics are shown in table 6-1. AV_{DD} = DV_{DD} = DV_{DD}_PFD = V_P = 3.0V to 3.6V, AGND = DGND = DGND_PFD = CPGND = 0 V, dBm referred to 50 Ω, T_A = -55 ℃ to 125 ℃, unless otherwise noted.

Table 6-1 BM7101MQRH electrical characteristics

Parameter	min	typ	max	Unit	Test conditions/comments
RF CHARACTERISTICS					
RF Input Frequency(RF_{IN})[1]	0.5	-	5.0	GHz	For lower frequencies, ensure slew rate (SR) > 320V/μS
RF Input Sensitivity	-5	-	5	dBm	
REF_{IN} CHARACTERISTICS					
REF_{IN} Input Frequency	10	-	200	MHz	For f<20MHz, ensure SR > 50V/μS, Biased at VDD/2.
REF_{IN} Input Sensitivity[2]	0.8	-	V_{DD}	Vp-p	
REF_{IN} Input Current	-100	-	100	uA	
PHASE DETECTOR					
Phase Detector Frequency	-	-	20	MHz	
PHASE DETECTOR OUTPUT					
PD_DN	-	-	20	MHz	

PD_UP	-	-	20	MHz	
LD_OUT	0.4	-	DV_{DD}-0.4	V	
CHARGE PUMP					
I_{CP} Sink/Source Value	-	2.5	-	mA	RSET=5.1KΩ
LOGIC INPUTS					
V_{IH}, Input High Voltage	2.0	-	-	V	
V_{IL}, Input Low Voltage	-	-	0.7	V	
I_{INH}, I_{INL}, Input Current	-100	-	100	uA	DV_{DD}=3.6V
LOGIC OUTPUTS					
V_{OH}, Output High Voltage	DV_{DD}-0.4	-	-	V	CMOS output, I_{OH}= -100uA
V_{OL}, Output Low Voltage	-	-	0.4	V	I_{OL}= 500uA
POWER SUPPLIES					
AV_{DD}=DV_{DD}_PFD=DV_{DD}	3.0	-	3.6	V	
VP	AV_{DD}	-	3.6	V	
I_{DD}		15		mA	TA=25℃, AV_{DD}=DV_{DD}_PFD=DV_{DD}=V_P=3.3V P=32, RF_{IN}=5.0GHz
NOISE CHARACTERISTICS					
Normalized Phase Noise Floor[3]	-	-219	-	dBc/Hz	
Phase Noise	-	-93	-	dBc/Hz	@10KHz offset,f_{PFD}=10MHz，@4.95GHz
	-	-82	-	dBc/Hz	@10KHz offse, f_{PFD}=1MHz，@4.95GHz
Spur	-	-67	-	dBc	@1MHz offse,f_{PFD}=1MHz，@4.95GHz
	-	-72	-	dBc	@2MHz offse,f_{PFD}=1MHz，@4.95GHz

Note1. If the minimum reference frequency and the RF input frequency of BM7101MQRH need to be less than 20MHz and 500MHz respectively, adding an additional clock buffer is necessary.

Note2. AC coupling ensures V_{DD}/2 bias.

Note3. The synthesizer phase noise floor is estimated by measuring the in-band phase noise at the output of the VCO and subtracting 20log N (where N = BP + A) and 10log f_{PFD}. PN_{SYNTH} = PN_{TOT} -10log f_{PFD}-20log N.

7. Notice

1) The RF and REF input signals need sufficient slew rate at different operating frequencies to ensure the dividers work correctly (SR $\geqslant 2\times\pi\times f\times V_P$, f is the input frequency, V_P is the input amplitude). For example, when the input frequency f is 500MHz and the input amplitude V_P is 0dBm, the slew rate SR needs to be larger than 942V/us.

In addition, the RF input stage is differential input. If a single input is used in application, unused input must be grounded with a capacitor, and the value must be the same as the DC-blocking capacitor at the used input.

2) The off-chip LPF directly affects the phase noise and lock time of the frequency synthesizer. In the case of low noise applications, the passive LPF is used to convert the charge pump output current into a control voltage usually. In the circuit design, it is recommended to use the third-order LPF to improve the suppression of spurious signals.

3) The MUXOUT port is only used to detect the internal signal state. When turned on, it may deteriorate the noise performance of the frequency synthesizer, and even cause the PLL to be loss of lock. When the PLL is working properly, the MUXOUT port should be set to the three-state output.

4) In the space environment, the single-event effect may cause functional interruptions of the device and cannot be automatically recovered. When the lock signal (LD_OUT) is low, the device needs to be reset through the CE port and refresh the register.

5) In application, the main characteristic parameters of the device, such as the PFD frequency, CP current and etc. should be designed and optimized with the characteristic parameters of off-chip VCO and LPF to ensure the frequency synthesizers work properly.

6) The bandwidth of off-chip LPF is between one tenth and one fifteen of the PFD frequency. When PFD frequency is too high, the bandwidth is out of this range that may cause the PLL to be loss of lock. The PFD frequency should be designed properly in application.

7) The RF input port and off-chip VCO output port should be impedance matched and the connection of these ports should be designed as short as possible.

8) The ripple of the power supply voltage will affect the working state of the device. When the voltage ripple is too large, the device may be loss of lock. Therefore,

it is recommended to use a low dropout regulator (LDO) as the power supply.

9) The power supply of the device, such as analog power supply (AV_{DD}), digital power supply (DV_{DD}), PFD power supply(DV_{DD}_PFD) and CP power supply (V_P), should have good decoupling. Decoupling capacitors should be placed as close as possible to those pins.

8. Typical Application

The circuit diagram of BM7101MQRH typical application is shown in figure 8-1. The reference input signal is applied to the circuit at $FREF_{IN}$ with a TCXO or another low noise frequency source. The third-order LPF output (The values of R and C are typical values in figure 8-1. That need to be optimized according to the condition of the PLL loop.) drives the VCO, which in turn is fed back to the RF input of the PLL synthesizer and also drives the RF output terminal. The MUXOUT pin can be programmed to monitor various internal signals in the synthesizer.

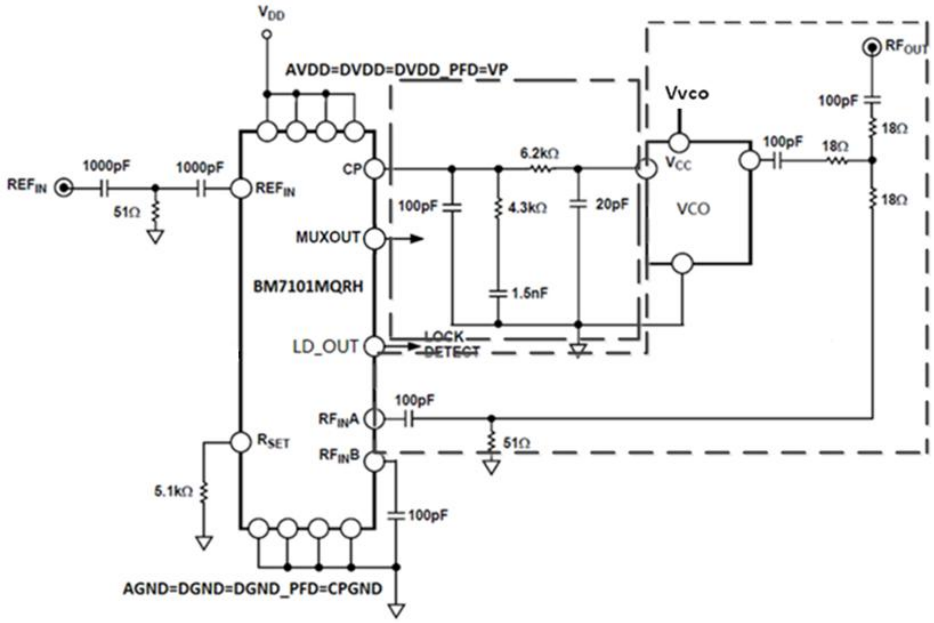

Figure 8-1 typical application circuit diagram

9. Package Specifications

The specifications of CQFP48 package are shown in figure7-1.

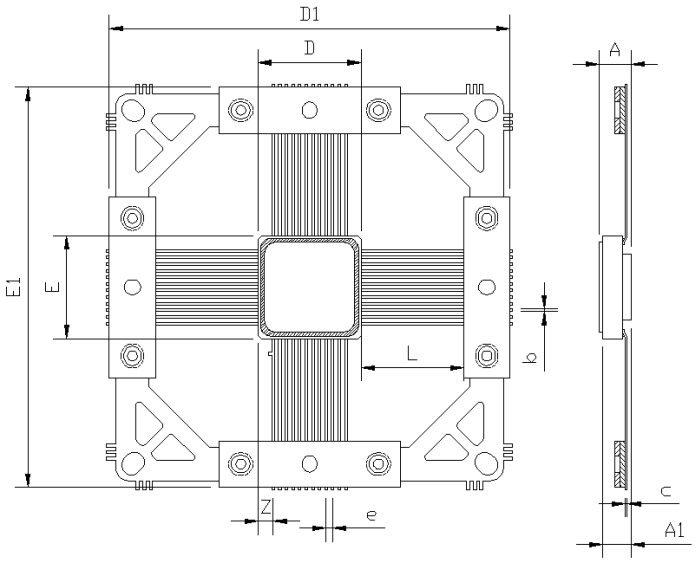

Figure 7-1 CQFP48 package specifications

Table 7-1 size symbol list

Size symbol	Value (unit: mm)		
	min	typical	max
A	2.1	——	2.7
A1	1.98	——	2.3
b	0.15	——	0.25
c	——	0.15	——
e	——	0.5	——
Z	——	1.15	——
D/E	7.6	7.8	8.0
D1/E1	30.0	——	30.6
L	——	7.75	——

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