Ver 1.0

3GHz Radiation hardened wideband integer-N frequency synthesizer

Datasheet

Part Number：B9702RH

北京微电子技术研究所

Beijing Microelectronics Technology Institute

Page of Revise Control

Version No.	Publish Time	Revised Chapter	Revise Introduction	Note
1.0	2018/03/07		Initial Revision	

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1. Features

- **Scrubbing features**
  - ÷10/11 dual modulus prescaler
  - Internal phase detector
  - Serial, parallel or hardwired programmable
  - Low phase noise
  - Compatible with PE9702
  - Package：44-lead CQFJ
- **Electrical characteristics**
  - 3.15V to 3.45V supply voltage
  - RF input frequency range : 0.5GHz ~ 3.0GHz
  - Reference input frequency range: ≤100MHz
- **Reliability features**
  - Operating temperature : -55℃ ～ +125℃
  - ESD(human body model) : 2000V
  - Total ionizing dose :
  - ≥100Krad(Si)
  - Single event latch-up threshold : ≥75MeV·cm^2/mg
  - Single event upset threshold : ≥37MeV·cm^2/mg

2. General Description

The B9702RH is a high performance integer-N PLL capable of frequency synthesizer up to 3GHz with superior phase noise performance. It features a 10/11 dual modulus prescaler, counters and a phase comparator as shown in Figure 3-1. Counter values are programmable through either a serial or parallel interface and can also be directly hard wired.

The B9702RH is optimized for space applications. Single Event Latch up (SEL) is better than 75MeV cm^2/mg, and Single Event Upset (SEU) is better than 37MeV cm^2/mg. It is offering excellent RF performance and intrinsic radiation tolerance. The normalized phase noise floor is -217dBc/Hz.

3. Function Block Diagram

B9702RH function block diagram is shown in figure 3-1.

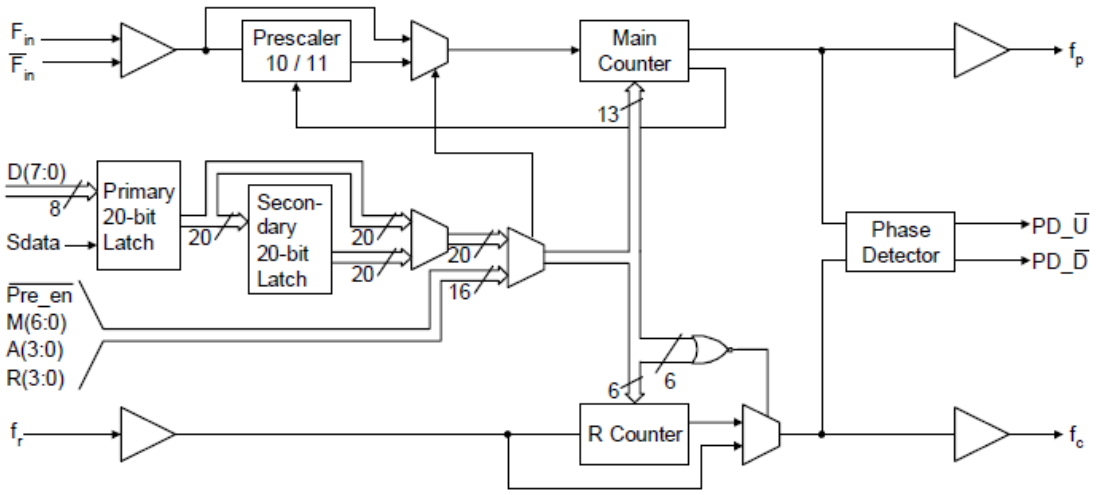

Figure 3-1 B9702RH function block digram

4. Packages and Pin Descriptions

The provided package is: 44-lead CQFJ.

B9702RH 44-lead CQFJ pin configuration is shown in Figure 4-1, in top view the pin P1 is in the middle of the up side, the pins are arranged in anticlockwise order.

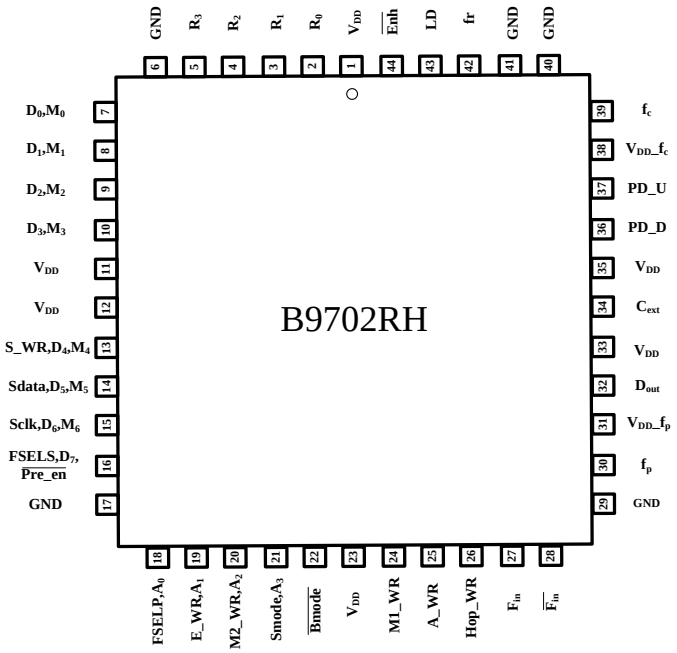

Figure 4-1 44-lead CQFJ pin configuration

Talble 4-1 B9702RH Pin Function Descriptions

Pin No.	Pin Name	Description	Interface Mode	Type
1	V_{DD}	Power supply input. Input may range from 3.15 V to 3.45 V. Bypassing recommended.	ALL	V_{DD}
2	R0	R counter bit0 (LSB)	Direct	I
3	R1	R counter bit1	Direct	I
4	R2	R counter bit2	Direct	I
5	R3	R counter bit3	Direct	I
6	GND	Ground	ALL	GND
7	D0	Parallel data bus bit0 (LSB)	Parallel	I
	M0	M counter bit0 (LSB)	Direct	I
8	D1	Parallel data bus bit1	Parallel	I
	M1	M counter bit1	Direct	I
9	D2	Parallel data bus bit2	Parallel	I
	M2	M counter bit2	Direct	I
10	D3	Parallel data bus bit3	Parallel	I
	M3	M counter bit3	Direct	I
11	V_{DD}	Same as pin1	ALL	V_{DD}
12	V_{DD}	Same as pin1	ALL	V_{DD}
13	S_WR	Serial load enable input. While S_WR is “low”, Sdata can be serially clocked. Primary register data is transferred to the secondary register on S_WR or Hop_WR rising edge.	Serial	I
	D4	Parallel data bus bit4	Parallel	I
	M4	M counter bit4	Direct	I
14	Sdata	Binary serial data input.Input data entered MSB first	Serial	I
	D5	Parallel data bus bit5	Parallel	I

	M5	M counter bit5	Direct	I
15	Sclk	Serial clock input. Sdata is clocked serially into the 20-bit primary register (E_WR“low”) or the 8-bit enhancement register (E_WR“high”) on the rising edge of Sclk.	Serial	I
	D6	Parallel data bus bit6	Parallel	I
	M6	M counter bit6	Direct	I
16	FSELS	Selects contents of primary register (FSELS=1) or secondary register (FSELS=0) for programming of internal counters while in Serial Interface Mode.	Serial	I
	D7	Parallel data bus bit7	Parallel	I
	$\overline{\text{Pre\_en}}$	Prescaler enable, active “low”. When “high”, Fin bypasses the prescaler.	Direct	I
17	GND	Ground	ALL	GND
18	FSELP	Selects contents of primary register (FSELP=1) or secondary register (FSELP=0) for programming of internal counters while in Parallel Interface Mode.	Parallel	I
	A0	A counter bit0 (LSB)	Direct	I
19	E_WR	Enhancement register write enable.While E_WR is “high”, Sdata can be serially clocked into the enhancement register on the rising edge of Sclk.	Serial	I
		Enhancement register write.D[7:0] are latched into the enhancement register on the rising edge of E_WR	Parallel	I
	A1	A counter bit1	Direct	I

20	M2_WR	M2 write. D[3:0] are latched into the primary register (R[5:4], M[8:7]) on the rising edge of M2_WR	Parallel	I
	A2	A counter bit2	Direct	I
21	Smode	Selects serial bus interface mode (Bmode=0, Smode=1) or Parallel Interface Mode (Bmode=0, Smode=0)	Serial,Parallel	I
	A3	A counter bit3 (MSB)	Direct	I
22	$\overline{\text{Bmode}}$	Selects direct interface mode (Bmode=1).	ALL	I
23	V_{DD}	Same as pin1	ALL	V_{DD}
24	M1_WR	M1 write. D[7:0] are latched into the primary register (Pre_en, M[6:0]) on the rising edge of M1_WR.	Parallel	I
25	A_WR	A write. D[7:0] are latched into the primary register (R[3:0], A[3:0]) on the rising edge of A_WR.	Parallel	I
26	Hop_WR	Hop write. The contents of the primary register are latched into the secondary register on the rising edge of Hop_WR.	Serial,Parallel	I
27	Fin	Prescaler input from the VCO.3.0 GHz max frequency	ALL	I
28	$\overline{\text{Fin}}$	Prescaler complementary input. A bypass capacitor in series with a 51 Ω resistor should be placed as close as possible to this pin and be connected directly to the ground plane.	ALL	I
29	GND	Ground	ALL	GND
30	fp	Monitor pin for main divider	ALL	O

		output. Switching activity can be disabled through enhancement register programming or by floating or grounding VDD pin 31.		
31	V_{DD}_fp	VDD for fp. Can be left floating or connected to GND to disable the fp output	ALL	V_{DD}
32	Dout	Data Out. The MSEL signal and the raw prescaler output are available on Dout	Serial,Parallel	O
33	V_{DD}	Same as pin 1	ALL	V_{DD}
34	Cext	Logical "NAND" of PD_U and PD_D terminated through an on chip, 2 kΩ series resistor. Connecting Cext to an external capacitor will low pass filter the input to the inverting amplifier used for driving LD	ALL	O
35	V_{DD}	Same as pin1	ALL	V_{DD}
36	PD_D	PD_D is pulse down when fp leads fc.	ALL	O
37	PD_U	PD_U is pulse down when fc leads fp.	ALL	O
38	V_{DD}_fc	VDD for fc. Can be left floating or connected to GND to disable the fc output.	ALL	V_{DD}
39	fc	Monitor pin for reference divider output. Switching activity can be disabled through enhancement register programming or by floating or grounding VDD pin 38	ALL	O
40	GND	Ground	ALL	GND
41	GND	Ground	ALL	GND
42	fr	Reference frequency input	ALL	I
43	LD	Lock detect and open drain	ALL	O

		logical inversion of CEXT. When the loop is in lock, LD is high impedance, otherwise LD is a logic low (“0”).		
44	$\overline{Enh}$	Enhancement mode. When asserted low (“0”), enhancement register bits are functional.	Serial,Parallel	I

5. Detailed Description

5.1 Function Description

The B9702RH consists of a prescaler, counters, a phase detector, and control logic. The dual modulus prescaler divides the VCO frequency by either 10 or 11, depending on the value of the modulus select. Counters “R” and “M” divide the reference and prescaler output, respectively, by integer values stored in a 20-bit register. An additional counter (“A”) is used in the modulus select logic. The phase-frequency detector generates up and down frequency control signals. The control logic includes a selectable chip interface. Data can be written via serial bus, parallel bus, or hardwired directly to the pins. There are also various operational and test modes and a lock detect output.

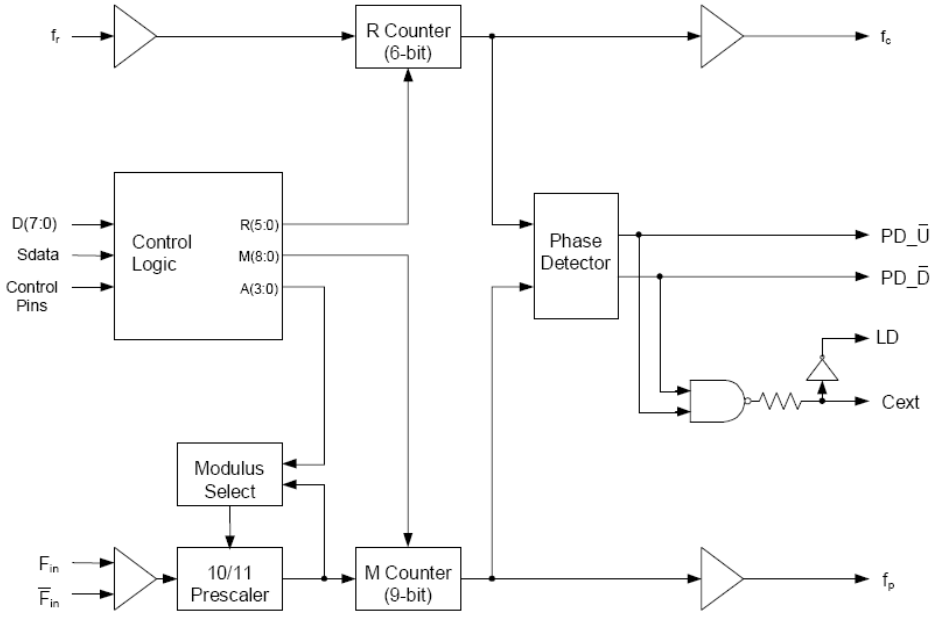

Figure 5-1 B9702RH function block diagram

1) Main Counter Chain

Normal Operating Mode

The main counter chain divides the RF input frequency, Fin, by an integer derived from the user-defined values in the "M" and "A" counters. It is composed of the 10/11 dual modulus prescaler, modulus select logic, and 9-bit M counter. Setting Pre_en "low" enables the 10/11 prescaler. Setting Pre_en "high" allows Fin to bypass the prescaler and powers down the prescaler. The output from the main counter chain, fp, is related to the VCO frequency, Fin, by the following equation:

$$f_P = F_{in} / \left[10 \times (M+1) + A\right]$$

where A ≤ M + 1, 1 ≤ M ≤ 511

When the loop is locked, Fin is related to the reference frequency, fr, by the following equation:

$$F_{in} = \left[10 \times (M+1) + A\right] \times \left(f_r / (R+1) \right)$$

where A ≤ M + 1, 1 ≤ M ≤ 511

A consequence of the upper limit on A is that Fin must be greater than or equal to 90 x (fr / (R+1)) to obtain contiguous channels. Programming the M Counter with the minimum value of "1" will result in a minimum M Counter divide ratio of "2".

In Direct Interface Mode, main counter inputs M7 and M8 are internally forced low. In this mode, the M value is limited to 1 ≤ M ≤ 127.

Prescaler Bypass Mode

Setting Pre_en "high" allows Fin to bypass and power down the prescaler. In this mode, the 10/11 prescaler and A register are not active, and the input VCO frequency is divided by the M counter directly. The following equation relates Fin to the reference frequency, fr:

$$F_{in} = (M+1) \times \left(f_r / (R+1) \right)$$

where 1 ≤ M ≤ 511

In Direct Interface Mode, main counter inputs M7 and M8 are internally forced low.In this mode, the M value is limited to 1 ≤ M ≤ 127.

2) Reference Counter

The reference counter chain divides the reference frequency, fr, down to the phase detector comparison frequency, fc. The output frequency of the 6-bit R Counter is related to the reference frequency by the following equation:

$$f_C = \left(f_r / (R+1) \right)$$

where 0 ≤ R ≤ 63

Note that programming R with "0" will pass the reference frequency, fr, directly to the phase detector.

In Direct Interface Mode, R Counter inputs R4 and R5 are internally forced low ("0"). In this mode, the R value is limited to 0 ≤ R ≤ 15.

3) Register Programming

Parallel Interface Mode

Parallel Interface Mode is selected by setting the Bmode input "low" and the Smode input "low". Parallel input data, D[7:0], are latched in a parallel fashion into one of three 8-bit primary register sections on the rising edge of M1_WR, M2_WR, or A_WR per the mapping shown in Table 5-1.The contents of the primary register are transferred into a secondary register on the rising edge of Hop_WR according to the timing diagram shown in Figure 5-2. Data is transferred to the counters as shown in Table 5-1.

The secondary register acts as a buffer to allow rapid changes to the VCO frequency. This double buffering for "ping-pong" counter control is programmed via the FSELP input. When FSELP is "high", the primary register contents set the counter inputs. When FSELP is "low", the secondary register contents are utilized. Parallel input data, D[7:0], are latched into the enhancement register on the rising edge of E_WR according to the timing diagram shown in Figure 5-2. This data provides control bits as shown in Table 5-2 with bit functionality enabled by asserting the $\overline{\text{Enh}}$ input "low".

Serial Interface Mode

Serial Interface Mode is selected by setting the Bmode input "low" and the Smode input "high". While the E_WR input is "low" and the S_WR input is "low", serial input data (Sdata input), B0 to B19, is clocked serially into the primary register on the rising edge of Sclk, MSB (B0) first. The contents from the primary register are transferred into the secondary register on the rising edge of either S_WR or Hop_WR according to the timing diagram shown in Figure 5-3. Data is transferred to the counters as shown in Table 5-1.

The double buffering provided by the primary and secondary registers allows for "ping-pong" counter control using the FSELS input. When FSELS is "high", the primary register contents set the counter inputs. When FSELS is "low", the secondary register contents are utilized. While the E_WR input is "high" and the S_WR input is "low", serial input data (Sdata input), B0 to B7, is clocked serially into the

enhancement register on the rising edge of Sclk, MSB (B0) first. The enhancement register is double buffered to prevent inadvertent control changes during serial loading, with buffer capture of the serially-entered data performed on the falling edge of E_WR according to the timing diagram shown in Figure 5-2.After the falling edge of E_WR, the data provides control bits as shown in Table 5-2 with bit functionality enabled by asserting the $\overline{Enh}$ input "low".

Direct Interface Mode

Direct Interface Mode is selected by setting the Bmode input "high".

Counter control bits are set directly at the pins as shown in Table 5-1.In Direct Interface Mode, main counter inputs M7 and M8, and R Counter inputs R4 and R5 are internally forced low ("0").

Table 5-1. Primary Register Programming

Interface Mode	$\overline{Enh}$	$\overline{Bmode}$	Smode	R_5	R_4	M_8	M_7	$\overline{Pre\_en}$	M_6	M_5	M_4	M_3	M_2	M_1	M_0	R_3	R_2	R_1	R_0	A_3	A_2	A_1	A_0
Parallel	1	0	0	M2_WR rising edge load				M1_WR rising edge load								A_WR rising edge load							
				D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Serial*	1	0	1	B_0	B_1	B_2	B_3	B_4	B_5	B_6	B_7	B_8	B_9	B_{10}	B_{11}	B_{12}	B_{13}	B_{14}	B_{15}	B_{16}	B_{17}	B_{18}	B_{19}
Direct	1	1	X	0	0	0	0	$\overline{Pre\_en}$	M_6	M_5	M_4	M_3	M_2	M_1	M_0	R_3	R_2	R_1	R_0	A_3	A_2	A_1	A_0

*Serial data clocked serially on Sclk rising edge while E_WR "low" and captured in secondary register on S_WR rising edge.

MSB (first in) (last in) LSB

Table 5-2. Enhancement Register Programming

Interface Mode	$\overline{Enh}$	$\overline{Bmode}$	Smode	Reserved	Reserved	Reserved	Power down	Counter load	MSEL output	Prescaler output	f_c, f_p OE
Parallel	0	0	0	E_WR rising edge load							
				D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Serial*	0	0	1	B_0	B_1	B_2	B_3	B_4	B_5	B_6	B_7

*Serial data clocked serially on Sclk rising edge while E_WR "high" and captured in the double buffer on E_WR falling edge.

MSB (first in) (last in) LSB

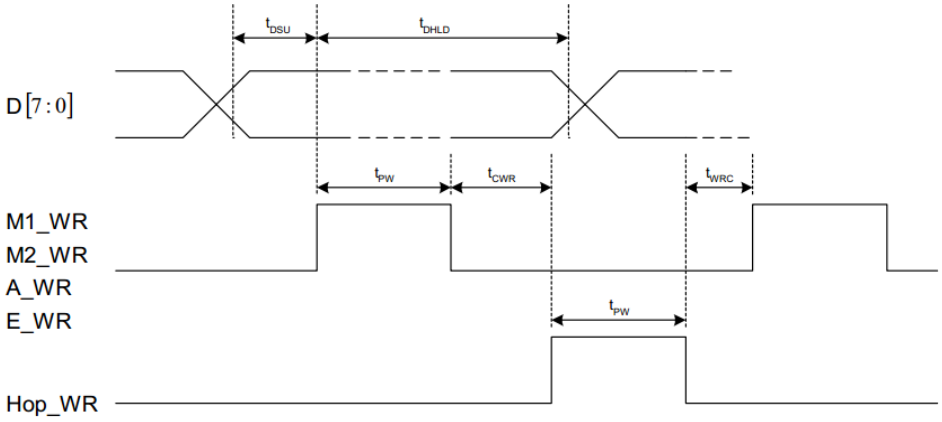

Figure 5-2. Parallel Interface Mode Timing Diagram

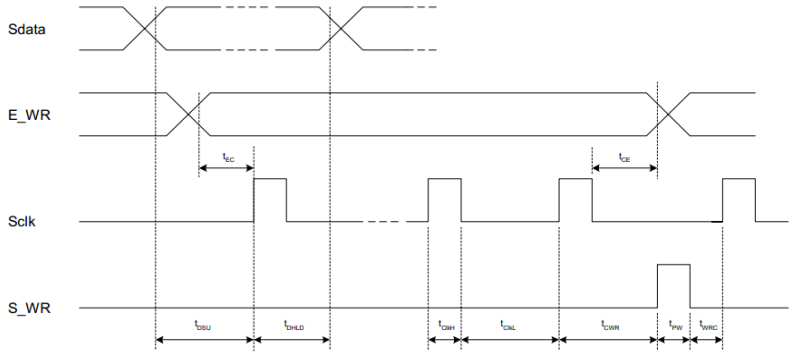

Figure 5-3. Serial Interface Mode Timing Diagram

4) Enhancement Register Bit Functionality

The functions of the enhancement register bits are shown below with all bits active high.

Table 5-3. Enhancement Register Bit Functionality

Bit function		Description
Bit 0	Reserved**	
Bit 1	Reserved**	
Bit 2	Reserved**	
Bit 3	Power down	Power down of all functions except programming interface.
Bit 4	MSEL output	Drives the internal dual modulus prescaler modulus select (MSEL)onto the Dout output.
Bit 5	Counter load	Immediate and continuous load of counter programming as directed by the Bmode and Smode inputs.
Bit 6	Prescaler output	Dirves the raw internal prescaler output(fmain)onto the Dout output.
Bit 7	f_p,f_c OE	f_p,f_c outputs disabled

**program to 0

5) Phase Dector

The phase detector is triggered by rising edges from the main Counter (fp) and the reference counter (fc). It has two outputs, namely PD_U, and PD_D. If the divided VCO leads the divided reference in phase or frequency (fp leads fc), PD_D pulses “low”. If the divided reference leads the divided VCO in phase or frequency (fr leads fp), PD_U pulses “low”. The width of either pulse is directly proportional to phase offset between the two input signals, fp and fc. The phase detector gain is 430 mV /

radian. PD_U and PD_D are designed to drive an active loop filter which controls the VCO tune voltage.

PD_U pulses result in an increase in VCO frequency and PD_D results in a decrease in VCO frequency. A lock detect output, LD is also provided, via the pin Cext. Cext is the logical "NAND" of PD_U and PD_D waveforms, which is driven through a series 2k ohm resistor. Connecting Cext to an external shunt capacitor provides integration. Cext also drives the input of an internal inverting comparator with an open drain output. Thus LD is an "AND" function of PD_U and PD_D. See Figure1 for a schematic of this circuit.

5.2 Storage Condition

Packaged product should be stored in the ventilate warehouse with ambient temperature 10℃～30℃ and relative humidity less than 70%. There should be no acid , alkali or other radiant gas in the environment.

5.3 Absolute Maximum Ratings

a) Supply voltage (V_{DD}) : -0.3 V ～ 3.9V
b) Voltage on any input (V_I) : -0.3 V ～ V_{DD}+0.3V
c) Operating temperature range (T_A) : -55℃～ 125℃
d) Storage temperature range (T_{stg}) : -65℃～ 150℃
e) Maximum Junction Temperature (T_J) : 150℃
f) Thermal resistance junction to case ($R_{th(J-C)}$) : 5℃/W
g) Lead temperature 10s (T_h) : 260℃

5.4 Recommended Operation Conditions

a) Supply voltage (V_{DD}) : 3.15V ~ 3.45V
b) Case operation temperature range (T_A) : -55℃ ~ 125℃

6. Specifications

All electrical characteristics are shown in table 6-1 and table 6-2. V_{DD}=3.3V, T_A = -55℃ to 125℃, unless otherwise noted.

Table 6-1 B9702RH DC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{dd}	Operational supply current	V_{DD}=3.15 to 3.45V				
	Prescaler disabled			15		mA
	Prescaler enabled			32	37	mA
Digital Inputs : All except f_r, F_{in},						
V_{IH}	High level input voltage	V_{DD}=3.15 to 3.45V	0.7×V_{DD}			V
V_{IL}	Low level input voltage	V_{DD}=3.15 to 3.45V			0.3×V_{DD}	V
I_{IH}	High level input current	V_{IH}=V_{DD}=3.45V			+70	uA
I_{IL}	Low level input current	V_{IL}=0, V_{DD}=3.45V	-1			uA
Reference Divider input: f_r						
I_{IHR}	High level input current	V_{IH}=V_{DD}=3.45V			+100	uA
I_{ILR}	Low level input current	V_{IL}=0, V_{DD}=3.45V	-100			uA
R0 Input: R_0						
I_{IHR}	High level input current	V_{IH}=V_{DD}=3.45V			+70	uA
I_{ILR}	Low level input current	V_{IL}=0, V_{DD}=3.45V	-5			uA
Counter and phase detector outputs: f_c , f_p						
V_{OLD}	Output voltage Low	I_{out}=6mA			0.4	V
V_{OHD}	Output voltage High	I_{out}=-3mA	V_{DD}-0.4			V
Lock detect outputs: Cext, LD						
V_{OLC}	Output voltage Low, Cext	I_{out}=100uA			0.4	V

V_{OHC}	Output voltage High, Cext	I_{out}=-100uA	V_{DD}-0.4			V
V_{OLLD}	Output voltage Low, LD	I_{out}=6mA			0.4	V

Table 6-2 B9702RH AC characteristics

Symbol	Parameter	Conditions	Min	Max	Units
Control interface and latches(see figure3-1, 5-2, 5-3)					
f_{clk}	Serial data clock frequency	Note1		10	MHz
t_{clkH}	Serial clock HIGH time		30		ns
t_{clkL}	Serial clock LOW time		30		ns
t_{DSU}	Sdata set-up time after Sclk rising edge, D[7:0] set-up time to M1_WR, M2_WR, A_WR, E_WR rising edge		10		ns
t_{DHLD}	Sdata hold time after Sclk rising edge, D[7:0] hold time to M1_WR, M2_WR, A_WR, E_WR rising edge		10		ns
t_{PW}	S_WR, M1_WR, M2_WR, A_WR, E_WR pulse width		30		ns
t_{CWR}	Sclk rising edge to S_WR rising edge.S_WR, M1_WR, M2_WR, A_WR falling edge to Hop_WR rising edge		30		ns
t_{CE}	Sclk falling edge to E_WR transition		30		ns
t_{WRC}	S_WR falling edge to Sclk rising edge. Hop_WR falling edge to S_WR, M1_WR, M2_WR, A_WR rising edge		30		ns
t_{EC}	E_WR transition to Sclk rising edge		30		ns
t_{MDO}	MSEL data out delay after Fin rising edge	C_L=12pf		8	ns
Main Divider(Including Prescaler)					
F_{in}	Operating frequency	-40℃ ~ 85℃ P_{RFIN}=0dBm~10dBm	500	3000	MHz

		-55℃ ~ 125℃ P_{RFIN}=-5dBm~5dBm	500	2600	MHz
Main Divider(Prescaler Bypassed)					
F_{in}	Operating frequency		50	300	MHz
P_{Fin}	Input level range	External AC coupling	-5	5	dBm
Reference Divider					
f_r	Operating frequency	Note3		100	MHz
P_{fr}	Reference input power(Note2)	Single-ended input	-2		dBm
Phase detector					
f_c	Comparison frequency	(Note3)		20	MHz

Note1: f_{clk} is verified during the functional pattern test. Serial programming sections of the functional pattern are clocked at 10 MHz to verify f_{clk}.

Note2: CMOS logic levels can be used to drive reference input if DC coupled. Voltage input needs to be a minimum of 0.5Vp-p.

Note3: Parameter is guaranteed through characterization only and is not tested.

7. Package Specifications

The specifications of 44-lead CQFJ package are shown in figure7-1.

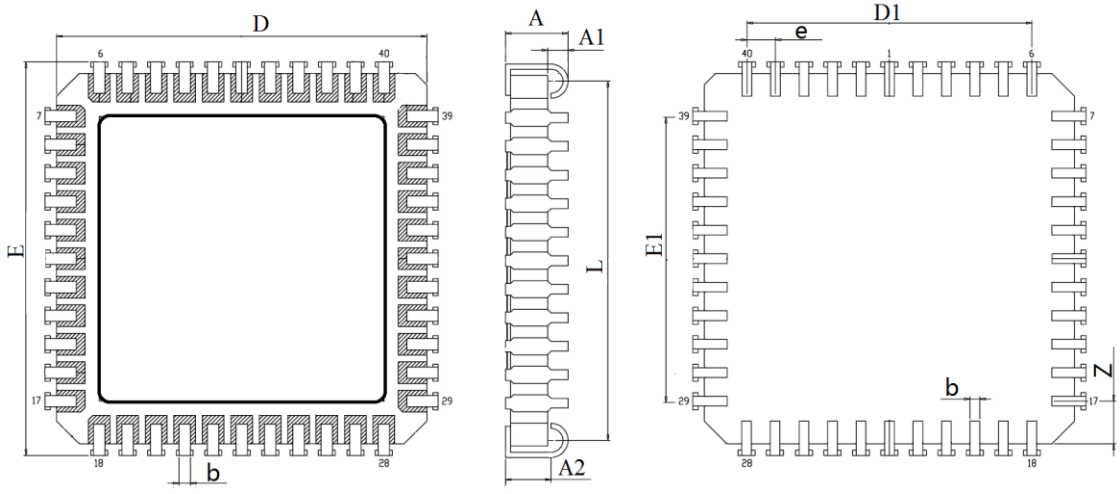

Figure 7-1 44-lead CQFJ package specifications

Table 7-1 size symbol list

Size symbol	Value (unit: mm)		
	min	typical	max
D/E	16.00	—	17.00
D1/E1	12.20	—	13.20
A	2.20	—	3.37
A1	0.56	—	1.26
A2	1.58	—	2.48
L	15.20	—	16.70
e	—	1.27	—
b	0.33	—	0.53
Z	1.45	—	2.35

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