

Ver 1.1

**Radiation-Hardened LVDS QUAD
RECEIVER**

Datasheet

Part Number: B54LVDS032RH



北京微电子技术研究所

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1. Features

- >155.5 Mbps (77.7 MHz) switching rates
- +340mV differential signaling
- 5 V power supply
- Cold Spare LVDS inputs
- TTL compatible outputs
- Ultra low power CMOS technology
- 8.0ns maximum propagation delay
- 3.0ns maximum differential skew
- Radiation-hardened design
 - Total-dose: 300 krad(Si)
 - Latchup (LET >75MeV-cm²/mg)
- Packaging options:
 - 16-lead flatpack (dual in-line)
- Compatible with IEEE 1596.3SCI LVDS
- Compatible with ANSI/TIA/EIA 644-1996 LVDS Standard

2. General Description

The B54LVDS032RH Quad Receiver is a quad CMOS differential line receiver designed for applications requiring ultra low power dissipation and high data rates. The device is designed to support data rates in excess of 155.5 Mbps (77.7 MHz) utilizing Low Voltage Differential Signaling (LVDS) technology.

The B54LVDS032RH accepts low voltage (340mV) differential input signals and translates them to 5V TTL output levels. The receiver supports a three-state function that may be used to multiplex outputs. The receiver also supports OPEN, shorted and terminated (100 Ω) input fail-safe. Receiver output will be HIGH for all fail-safe conditions.

The B54LVDS032RH and companion quad line driver B54LVDS031RH provides new alternatives to high power pseudo-ECL devices. All LVDS pins have Cold Spare buffers. These buffers will be high impedance when VDD is tied to VSS.

3. Function Block Diagram

B54LVDS032RH function block diagram is shown in figure 3-1.

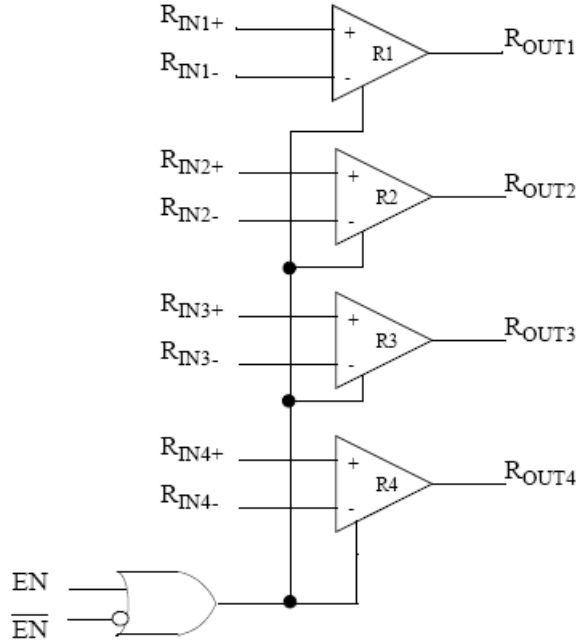


Figure 3-1 B54LVDS032RH Quad Receiver Block Diagram

4. Packages and Pin Function Descriptions

The provided package is: FP16

B54LVDS032RH pin configuration is shown in 4-1.

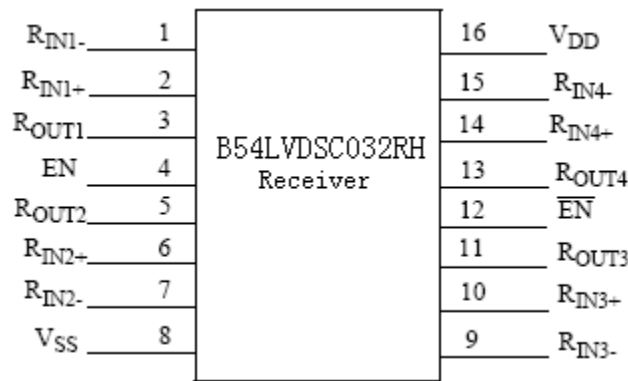


Figure 4-1 B26C32CERH pin configuration

Table 4-1 B26C32CERH Pin Function Descriptions

Pin No.	Name	Description
1, 7, 9, 15	$R_{IN1-}, R_{IN2-}, R_{IN3-}, R_{IN4-}$	Inverting receiver input pin
2, 6, 10, 14	$R_{IN1+}, R_{IN2+}, R_{IN3+}, R_{IN4+}$	Non-inverting receiver input pin
3, 5, 11, 13	$R_{OUT1}, R_{OUT2}, R_{OUT3}, R_{OUT4}$	Receiver output pin
4	ENABLE	Active high enable pin
12	\overline{EN}	Active low enable pin
16	V_{DD}	Power supply pin
8	V_{SS}	Ground pin

5. Pin List

B54LVDSV032RH- pin list is shown in table 5-1.

Table 5-1 B54LVDSV032RH- pin list

Pin No	Name	Description	Pin No.	Name	Description
1	R_{IN1-}	Inverting receiver input pin	9	R_{IN3-}	Inverting receiver input pin
2	R_{IN1+}	Non-inverting receiver input pin	10	R_{IN3+}	Non-inverting receiver input pin
3	R_{OUT1-}	Receiver output pin	11	R_{OUT3}	Receiver output pin
4	EN	Active high enable pin, OR-ed with \overline{EN}	12	\overline{EN}	Active low enable pin, OR-ed with EN
5	R_{OUT2}	Receiver output pin	13	R_{OUT4}	Receiver output pin
6	R_{IN2+}	Non-inverting receiver input pin	14	R_{IN4+}	Non-inverting receiver input pin
7	R_{IN2-}	Inverting receiver input pin	15	R_{IN4-}	Inverting receiver input pin
8	V_{SS}	Ground pin	16	V_{DD}	Power supply pin, +5V + 10%

6. Detailed Description

6.1 Truth Table

Table 6-1 truth table

Enables		Input	Output
EN	\overline{EN}	$R_{IN+}-R_{IN-}$	R_{OUT}
L	H	X	Z
All other combinations of ENABLE inputs		$V_{ID} \geq 0.1V$	H
		$V_{ID} \leq -0.1V$	L
		Full Fail-safe OPEN/SHORT or Terminated	H

L = Low logic state

X = Irrelevant

H = High logic state

Z = TRI-STATE (high impedance)

6.2 Timing Diagrams

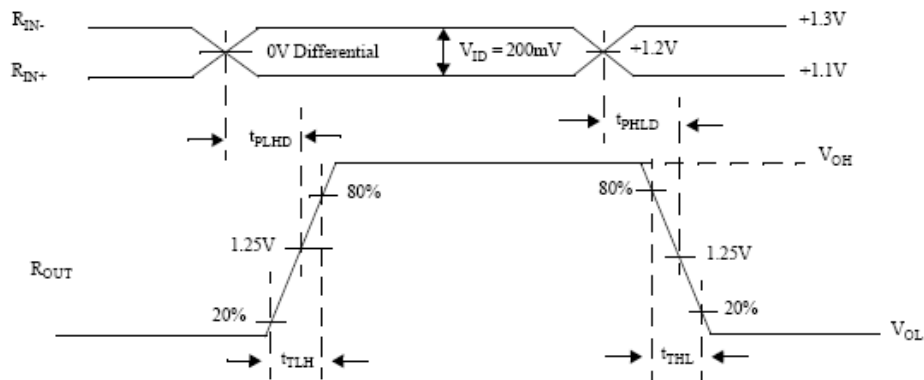


Figure 6-1 Receiver Propagation Delay and Transition Time Waveforms

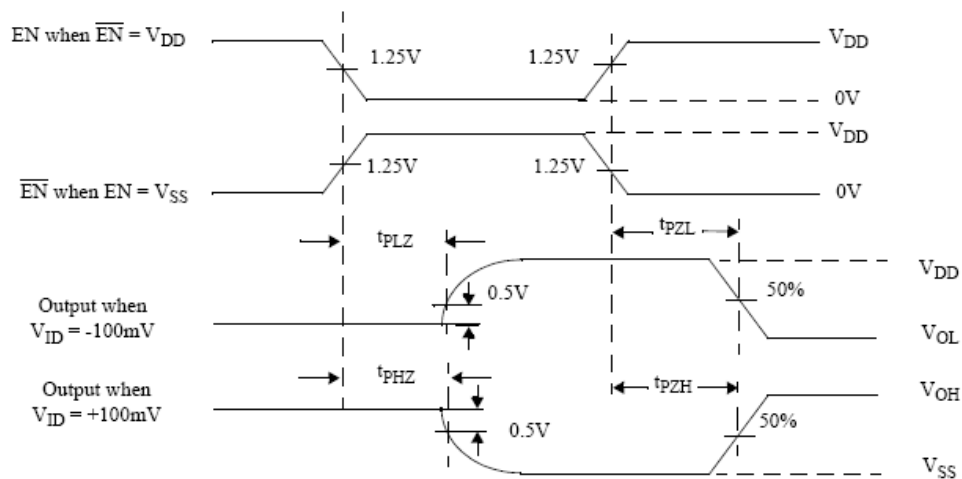


Figure 6-2 Receiver Three-State Delay Waveform

6.3 Storage Condition

Packaged product should be stored in the ventilate warehouse with ambient temperature $15^{\circ}\text{C} \sim 25^{\circ}\text{C}$ and relative humidity less than 65%. There should be no acid, alkali or other radiant gas in the environment.

6.4 Absolute Maximum Ratings

- Supply voltage (V_{DD}) : $-0.3\text{ V} \sim +6.0\text{V}$
- DC input voltage range (V_{in}) : $-0.3\text{V} \sim V_{DD} + 0.3\text{V}$
- Storage temperature (T_{stg}) : $-65^{\circ}\text{C} \sim +150^{\circ}\text{C}$
- Lead temperature ($T_H, 10\text{s}$) : 260°C
- Junction temperature (T_J): 150°C

6.5 Recommended Operation Conditions

- Supply Voltage (V_{DD}): $4.5\text{ V} \sim 5.5\text{ V}$
- DC input voltage, receiver inputs: 2.4V
- DC input voltage, logic inputs: 0 to V_{DD} for EN, \overline{EN}
- Case operation temperature range(T_A) : $-55^{\circ}\text{C} \sim 125^{\circ}\text{C}$

7. Specifications

All electrical characteristics are shown in table 7-1, Propagation Delay and Transition Time Waveforms are shown in Figure 7-1, Three-State Delay Waveform is shown in Figure 7-2.

Table 7-1 B26C32CERH electrical characteristics

DC ELECTRICAL CHARACTERISTICS¹

PARAMETER	SYM BOL	CONDITION (VDD = 5.0V ±10%; -55°C < TC < +125°C)	LIMITS		UNIT
			MIN	MAX	
High-level input voltage	V _{IH}	(TTL)	2.0	V _{DD}	V
Low-level input voltage	V _{IL}	(TTL)	GND	0.8	V
High-level output voltage	V _{OH}	I _{OH} = -0.4mA, V _{DD} = 4.5V	4.0	—	V
Low-level output voltage	V _{OL}	I _{OL} = 2mA, V _{DD} = 4.5V	—	0.3	V
Logic input leakage current	I _{IN}	Inputs V _{IN} = 0 and 2.4, V _{DD} =5.5V	-10	10	μA
		Enables EN/ \overline{EN} = 0 and 5.5V, V _{DD} =5.5V	-10	10	μA
Cold Spare Leakage LVDS Inputs	I _{CS}	V _{IN} =5.5V, V _{DD} =0V	-10	10	μA
Differential Input High Threshold	V _{TH} ³	V _{CM} = +1.2V	—	100	mV
Differential Input Low Threshold	V _{TL} ³	V _{CM} = +1.2V	-100	—	mV
Input clamp voltage	V _{CL}	I _{CL} = -18 mA	-1.5	—	V
Output Short Circuit Current	I _{OS} ³	Enabled, V _{OUT} =0V	-130	-15	mA
Output Three-State Current	I _{OZ} ⁴	Disabled, EN=0V, \overline{EN} =5V, V _{OUT} =0V or V _{DD} , V _{DD} =5.5V	-10	10	μA
Loaded supply current receivers enabled	I _{CC} ⁴	EN= \overline{EN} =0V or V _{DD} , IutputS Open	—	11.0	mA
Loaded supply current receivers disabled	I _{CCZ} ⁴	EN=0V, \overline{EN} =V _{DD} , IutputS Open	—	11.0	mA

Notes:

1. Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground.
2. Output short circuit current (IOS) is specified as magnitude only, minus sign indicates direction only. Only one output should be shorted at a time, do not exceed maximum junction temperature specification.
3. Guaranteed by characterization.
4. Device tested at VCC = 5.5V only.

AC SWITCHING CHARACTERISTICS^{1, 2, 3, 4}

PARAMETER	<i>SYMB OL</i>	CONDITION(VDD = 5.0V ±10%, TA = -55°C to +125°C)	MIN	MAX	UNIT
Functional Test		$f=77.7\text{MHz}$, $V_{DD}=4.5\text{V}$			
Differential Propagation Delay High to Low	t_{PHLD}	$C_L = 20\text{pf}$ (figures 6-1 and 7-1)	—	8.0	ns
Differential Propagation Delay Low to High	t_{PLHD}	$C_L = 20\text{pf}$ (figures 6-1 and 7-1)	—	8.0	ns
Differential Skew (tPHLD - tPLHD)	t_{SKD}		—	3.0	ns
Channel-to-Channel Skew ¹	t_{SK1} ⁴		—	3.0	ns
Chip-to-Chip Skew ⁵	t_{SK2} ⁴		—	7.0	ns
Disable Time High to Z	t_{PHZ} ⁴	(figures 6-2 and 7-2)	—	20	ns
Disable Time Low to Z	t_{PLZ} ⁴	(figures 6-2 and 7-2)	—	20	ns
Enable Time Z to High	t_{PZH} ⁴	(figures 6-2 and 7-2)	—	20	ns
Enable Time Z to Low	t_{PZL} ⁴	(figures 6-2 and 7-2)	—	20	ns

Notes:

1. Channel-to-Channel Skew is defined as the difference between the propagation delay of the channel and the other channels in the same chip with an event on the inputs.
2. Generator waveform for all tests unless otherwise specified: $f = 1\text{ MHz}$, $Z_0 = 50\Omega$, t_r and t_f (0% - 100%) < 1ns for RIN and t_r and t_f < 6ns for EN or EN.
3. C_L includes probe and jig capacitance.
4. Guaranteed by characterization.
5. Chip to Chip Skew is defined as the difference between the minimum and maximum specified differential propagation delays.

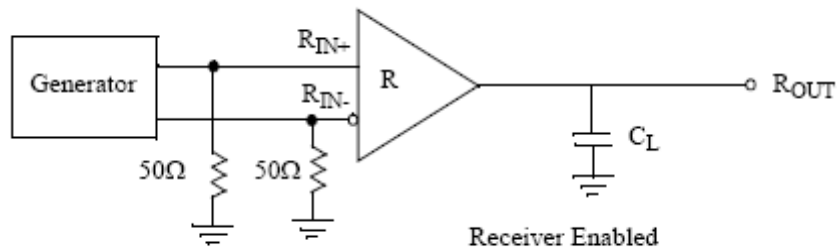


Figure 7-1. Receiver Propagation Delay and Transition Time Test Circuit or Equivalent Circuit

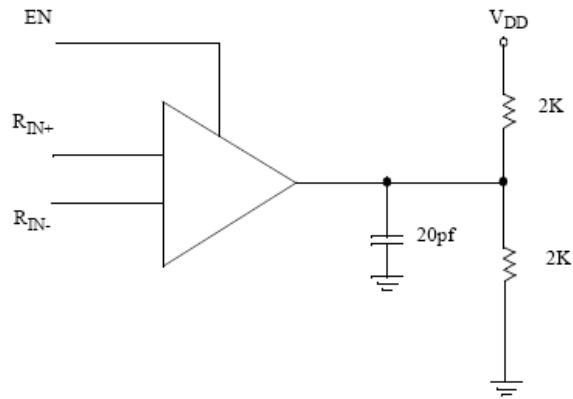


Figure 7-2. Receiver Three-State Delay Test Circuit or Equivalent Circuit

8. Package Specifications

B54LVDS032RH adopt 16-Lead Ceramic Quad Flat package, as in Figure 8-1 and the size is listed in Table 8-1.

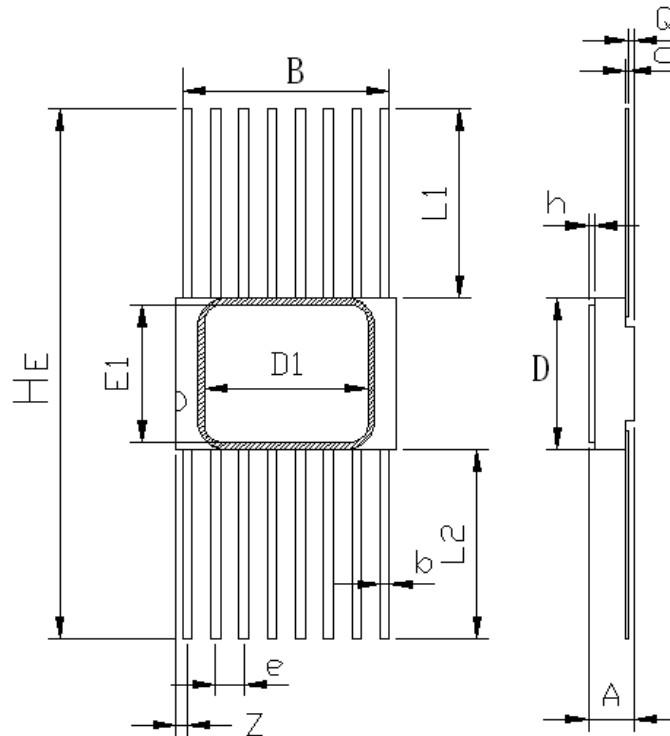


Figure.8-1. 16-pin Ceramic Flatpack

Table 8-1 Flat Package Size

Symbol	Value (unit: mm)		
	Min	Normal	Max
A	1.60	—	2.50
B	8.94	—	9.69
b	0.25	—	0.54
c	0.07	—	0.20
D	6.55	—	7.25
e	—	1.27	—
He	18.76	19.41	20.06
Q	0.13	—	0.90
L1	5.75	—	6.75
L2	5.75	—	6.75
Z	—	—	1.27
D1	—	7.366	—
E1	—	6.223	—
h	0.22	—	0.28

9. Appendix II Typical Application Example

The B54LVDS032RH receiver's intended use is primarily in an uncomplicated point-to-point configuration as is shown in Figure 9-1. This configuration provides a clean signaling environment for quick edge rates of the drivers. The receiver is connected to the driver through a balanced media which may be a standard twisted pair cable, a parallel pair cable, or simply PCB traces. Typically, the characteristic impedance of the media is in the range of 100Ω. A termination resistor of 100Ω should be selected to match the media and is located as close to the receiver input pins as possible. The termination resistor converts the current sourced by the driver into voltages that are detected by the receiver. Other configurations are possible such as a multi-receiver configuration, but the effects of a mid-stream connector(s), cable stub(s), and other impedance discontinuities, as well as ground shifting, noise margin limits, and total termination loading must be taken into account.

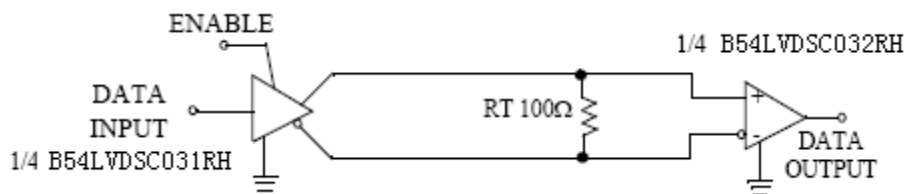


Figure 9-1. Point-to-Point Application

The B54LVDS032RH differential line receiver is capable of detecting signals as low as 100mV, over a $\pm 1V$ common-mode range centered around +1.2V. This is related to the driver offset voltage which is typically +1.2V. The driven signal is centered around this voltage and may shift $\pm 1V$ around this center point. The $\pm 1V$ shifting may be the result of a ground potential difference between the driver's ground reference and the receiver's ground reference, the common-mode effects of coupled noise or a combination of the two. Both receiver input pins should honor their specified operating input voltage range of 0V to +2.4V (measured from each pin to ground).

The B54LVDS032RH receiver is a high gain, high speed device that amplifies a small differential signal (20mV) to TTL logic levels. Due to the high gain and tight threshold of the receiver, care should be taken to prevent noise from appearing as a valid signal. The receiver's internal fail-safe circuitry is designed to source/sink a small amount of current, providing fail-safe protection (a stable known state of HIGH output voltage) for floating, terminated or shorted receiver inputs.

1. Open Input Pins. The B54LVDS032RH is a quad receiver device, and if an application requires only 1, 2 or 3 receivers, the unused channel(s) inputs should be left OPEN. Do not tie unused receiver inputs to ground or any other voltages. The input is

biased by internal high value pull up and pull down resistors to set the output to a HIGH state. This internal circuitry will guarantee a HIGH, stable output state for open inputs.

2. Terminated Input. If the driver is disconnected (cable unplugged), or if the driver is in a three-state or poweroff condition, the receiver output will again be in a HIGH state, even with the end of cable 100Ω termination resistor across the input pins. The unplugged cable can become a floating antenna which can pick up noise. If the cable picks up more than 10mV of differential noise, the receiver may see the noise as a valid signal and switch. To insure that any noise is seen as common-mode and not differential, a balanced interconnect should be used. Twisted pair cable offers better balance than flat ribbon cable.

3. Shorted Inputs. If a fault condition occurs that shorts the receiver inputs together, thus resulting in a 0V differential input voltage, the receiver output remains in a HIGH state. Shorted input fail-safe is not supported across the common-mode range of the device (VSS to 2.4V). It is only supported with inputs shorted and no external common-mode voltage applied.

10. Appendix I Replaced Product

Appendix table1-1

Device Type	Substituted Device Type
B54LVDSC032RH	UT54LVDSC032

Service and Support:

Address: No.2 Siyingmen N. Road. Donggaodi. Fengtai District.Beijing.China.

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